

1/34

Fig.1
PRIOR ART

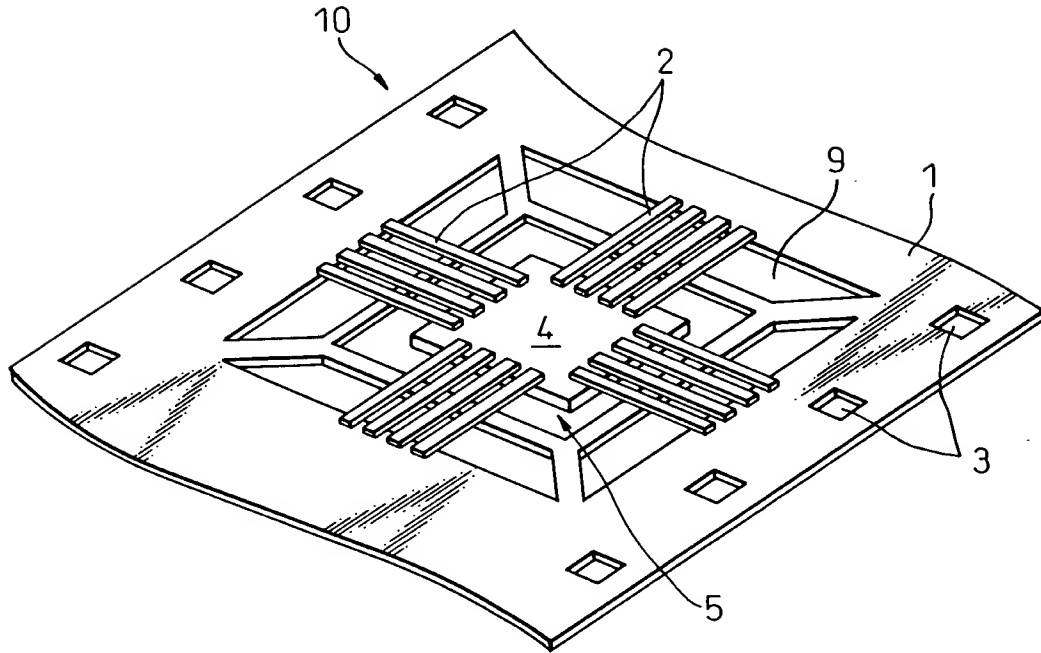


Fig.2
PRIOR ART

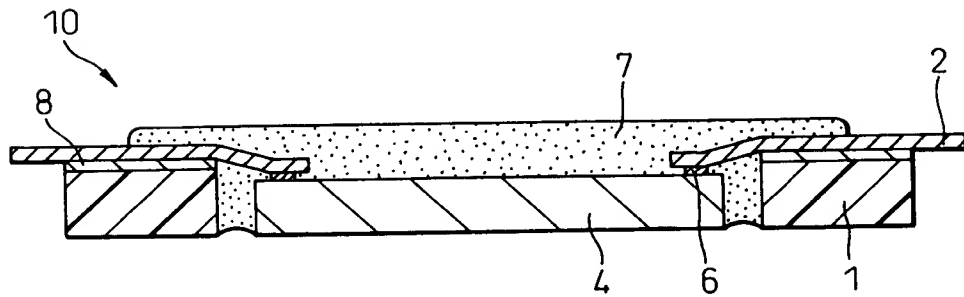
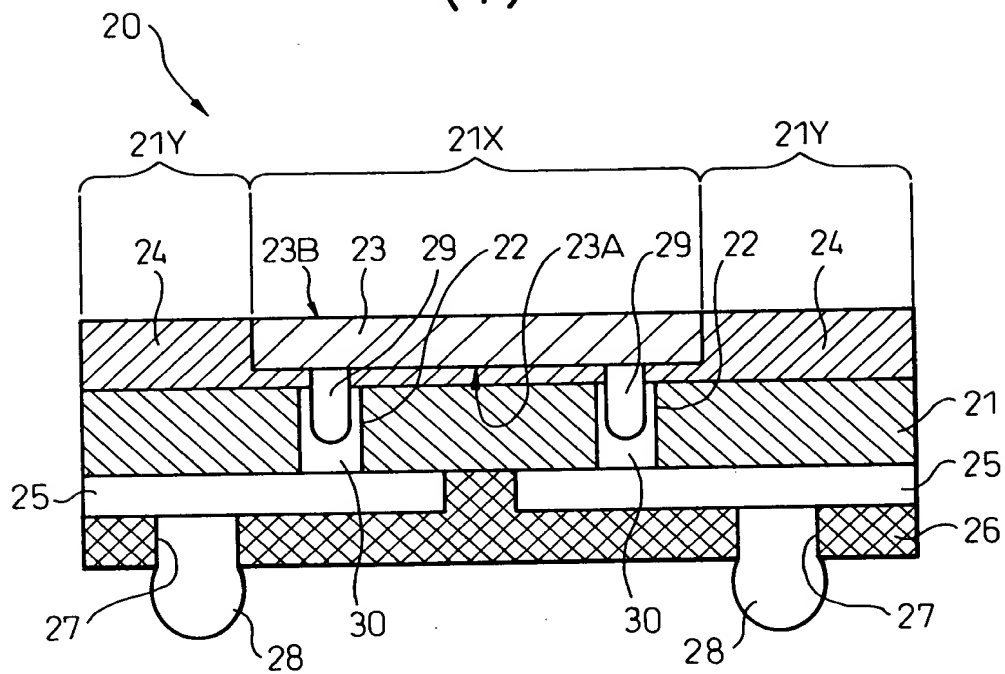


Fig.3
(1)



(2)

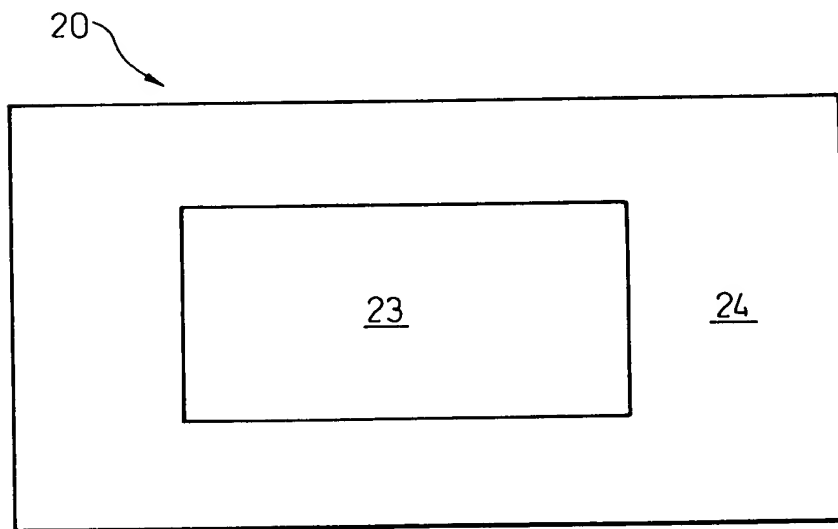


Fig. 4 is a cross-sectional view of the device of Fig. 1, taken along the line 4-4 of Fig. 1, showing the device in a second state of operation. In this state, the device is in a second state of operation, and the device is in a second state of operation.

Fig. 4

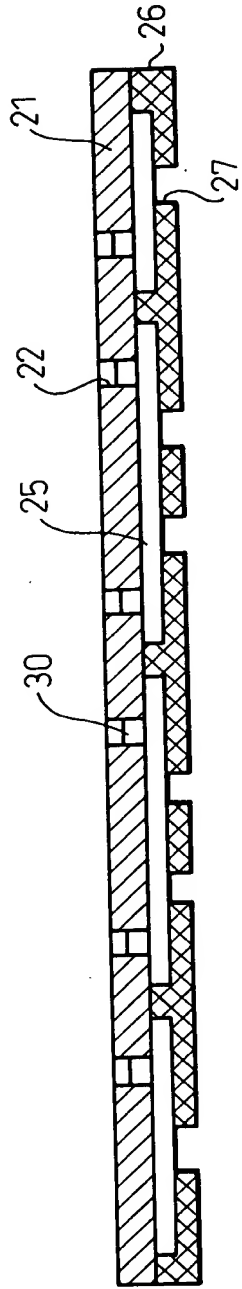
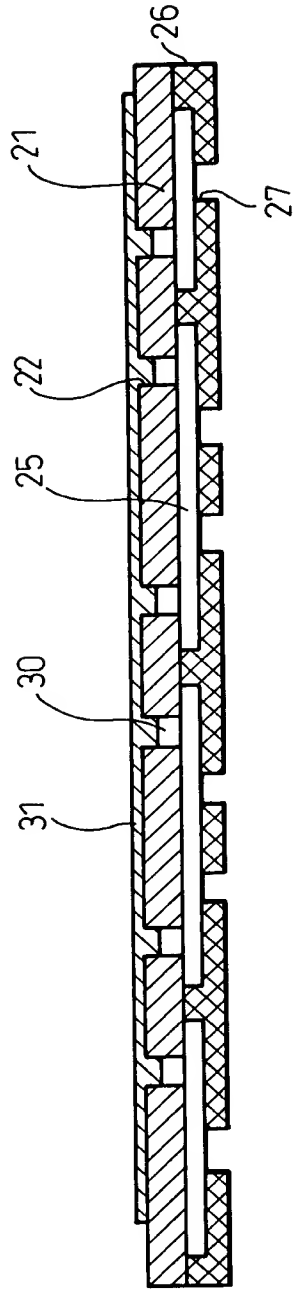


Fig.5



6. 5. 11

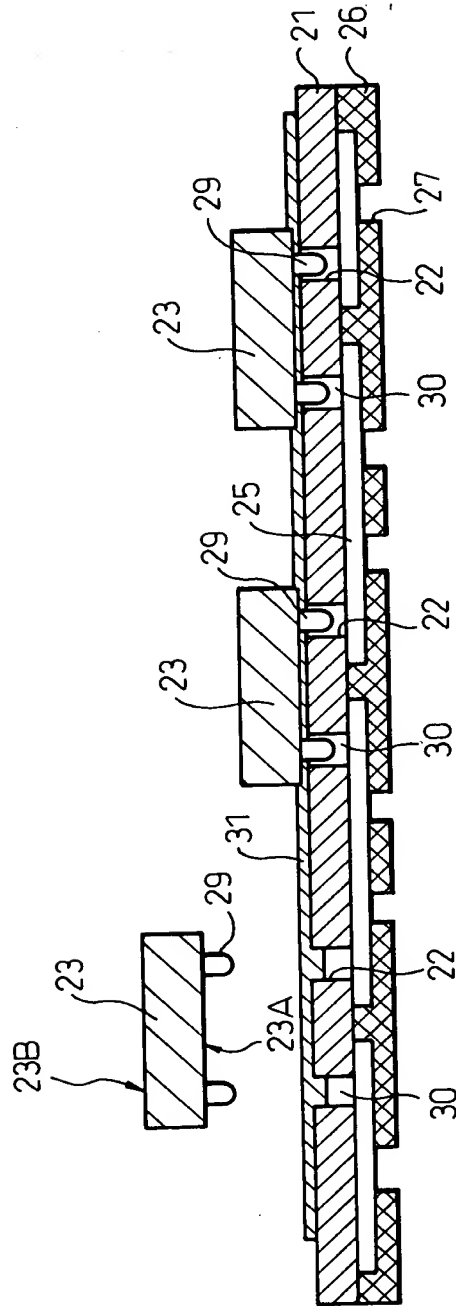


Fig. 7

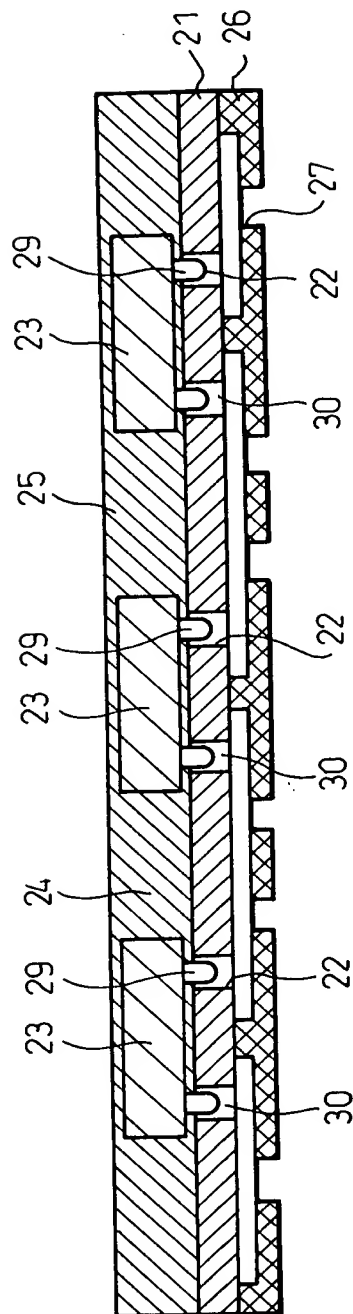
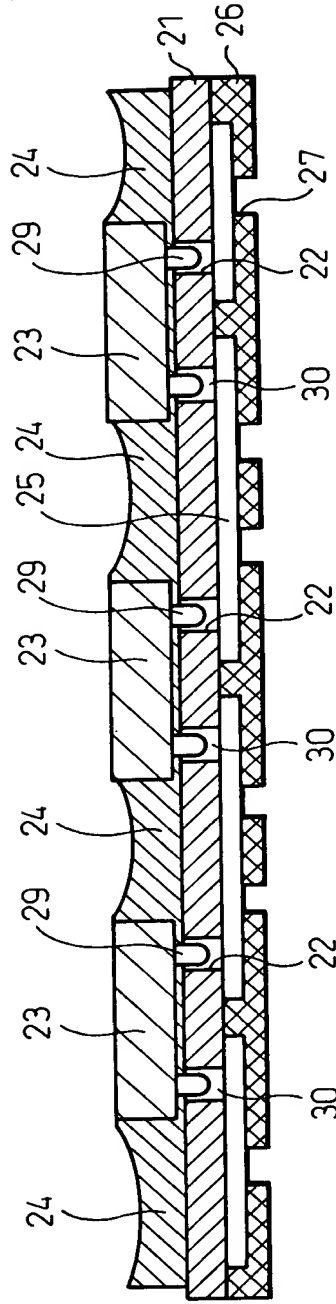


Fig. 8



உ.ர.ச.

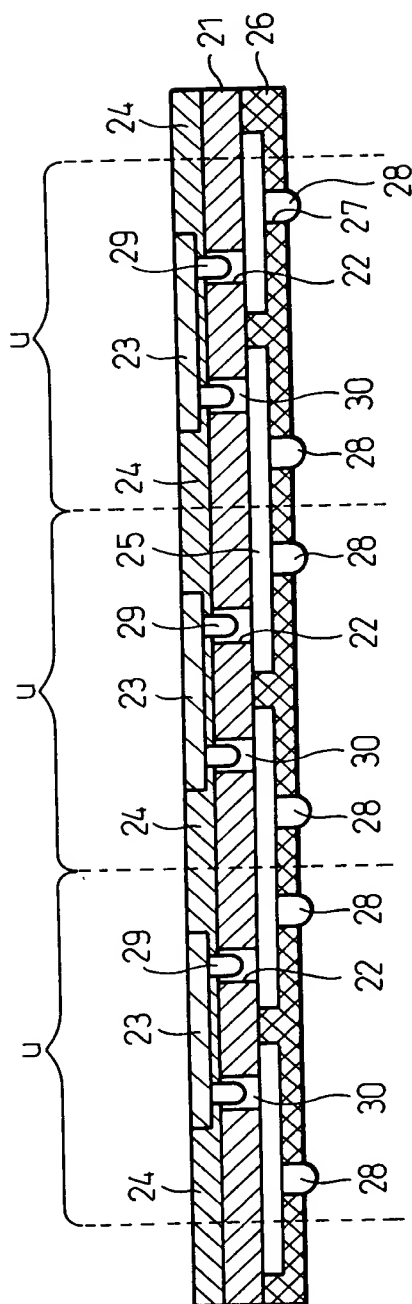
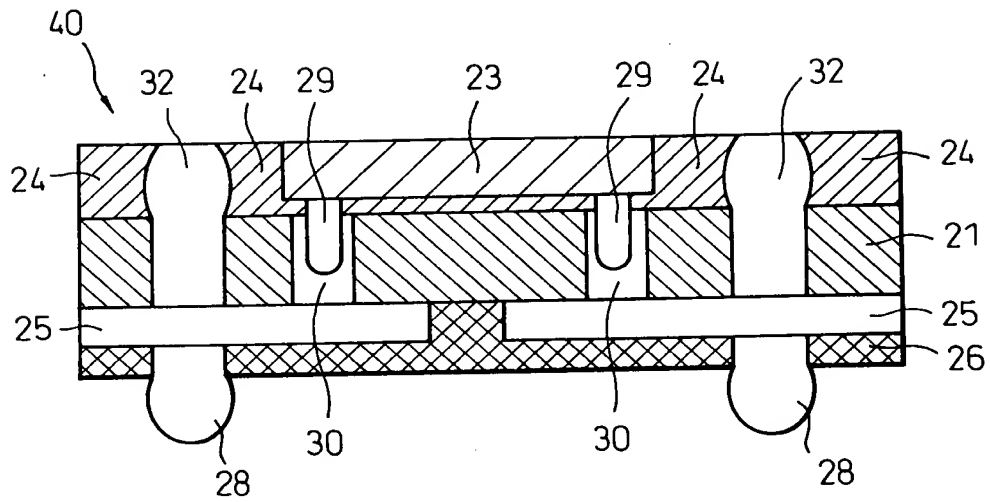


Fig.10

(1)



(2)

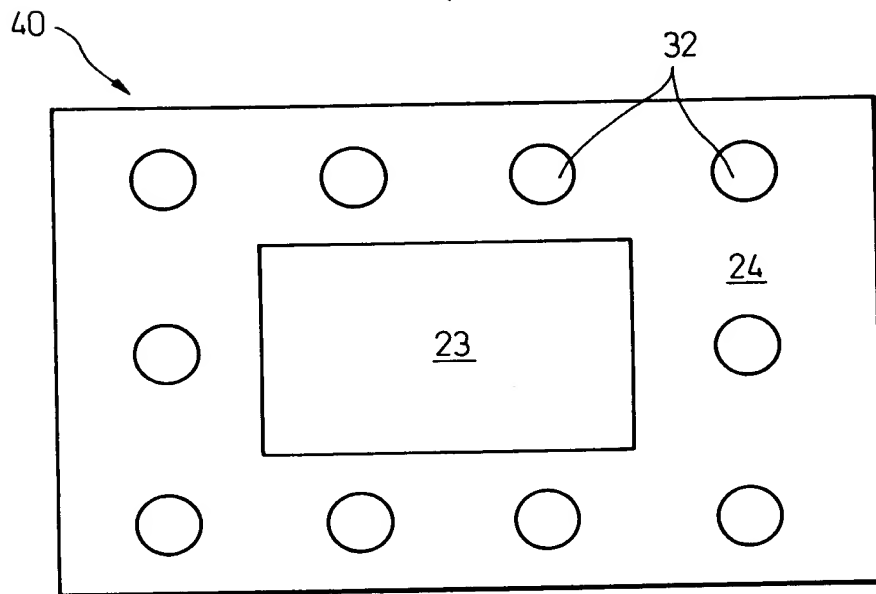


Fig.11

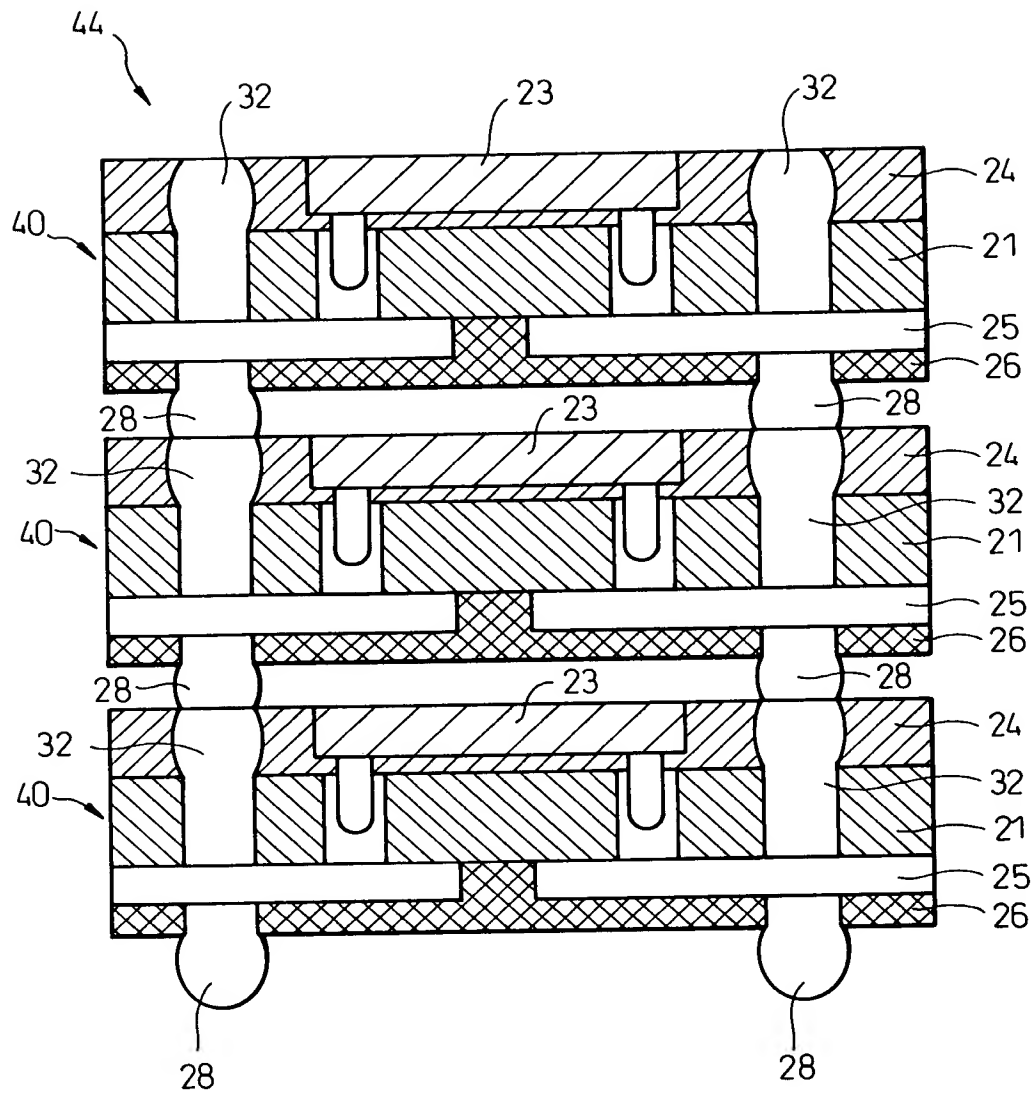


Fig. 11 is a cross-sectional view of the device of Fig. 10, taken along line 11-11 of Fig. 10, showing the device in a second state of operation. In this state, the device is in a retracted position, and the piston 22 is moved to the left, compressing the spring 24. The piston 22 is shown in a cross-hatched pattern, and the spring 24 is shown in a diagonal line pattern. The device is shown in a cross-sectional view, with the piston 22 and the spring 24 being the main components. The device is shown in a retracted position, and the piston 22 is moved to the left, compressing the spring 24. The piston 22 is shown in a cross-hatched pattern, and the spring 24 is shown in a diagonal line pattern. The device is shown in a cross-sectional view, with the piston 22 and the spring 24 being the main components.

Fig. 12

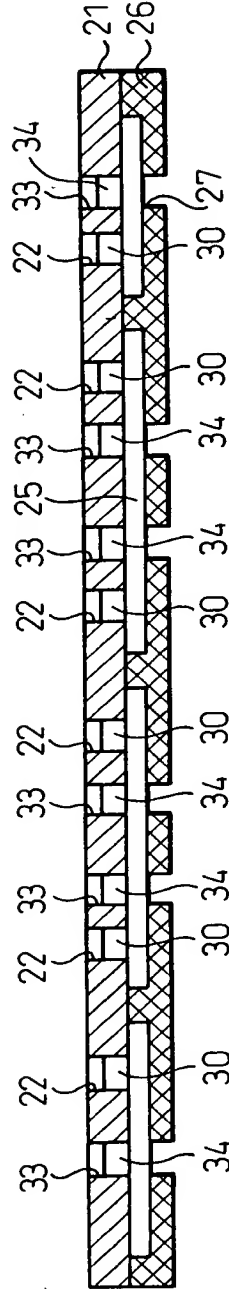


Fig. 13

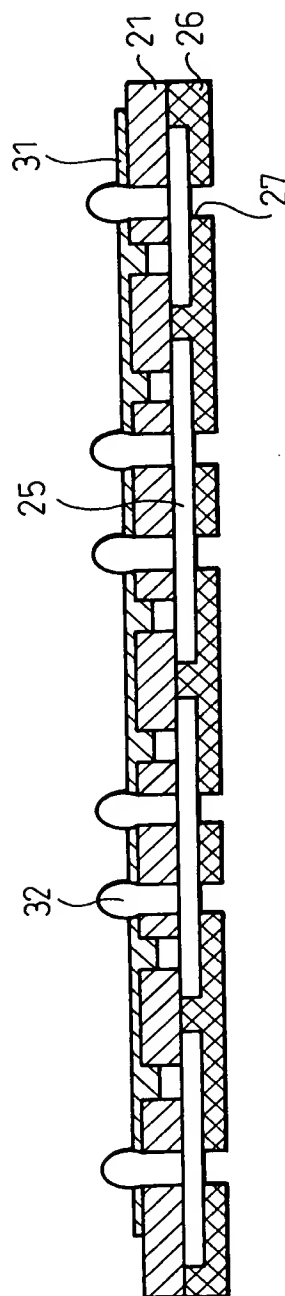


Fig.14

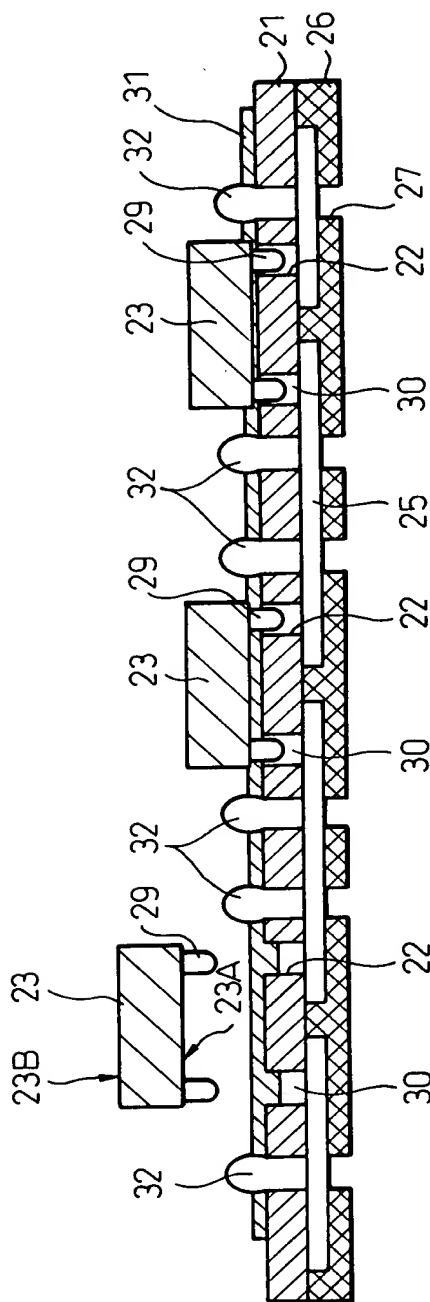


FIG. 15 is a cross-sectional view of the device of FIG. 14, showing the device in a second state. In this state, the device is in a second state, and the device is in a second state.

Fig.15

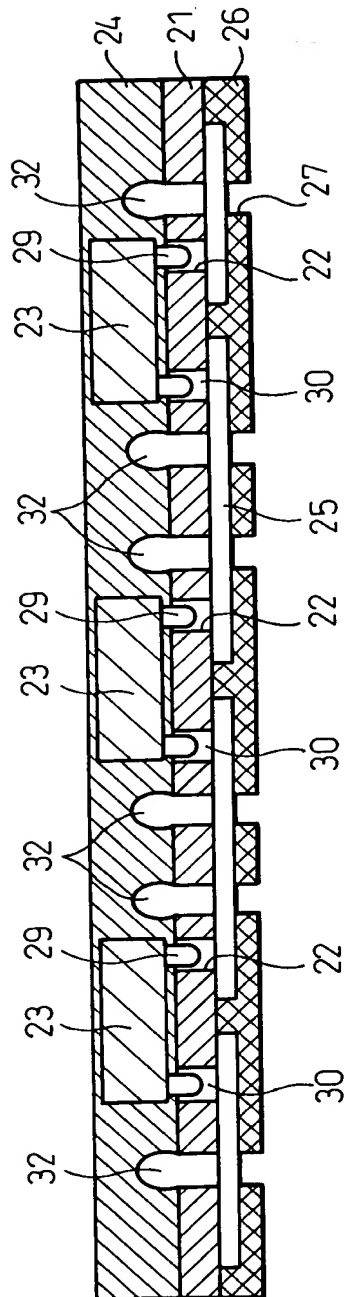


Fig.16

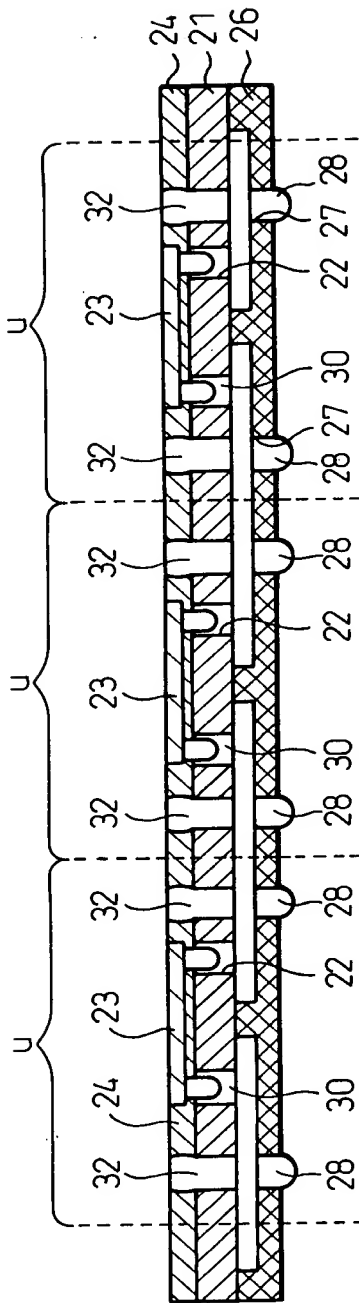
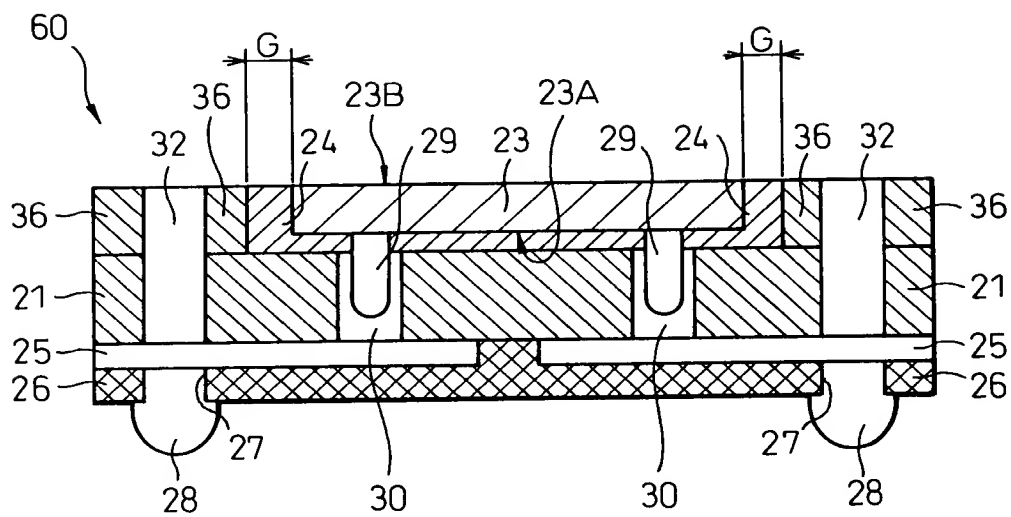


Fig.17

(1)



(2)

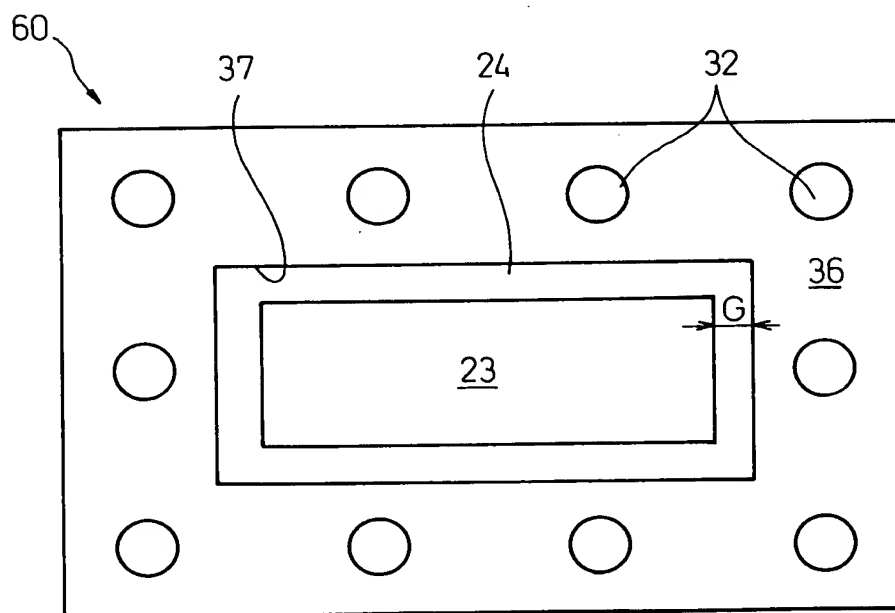


Fig.18

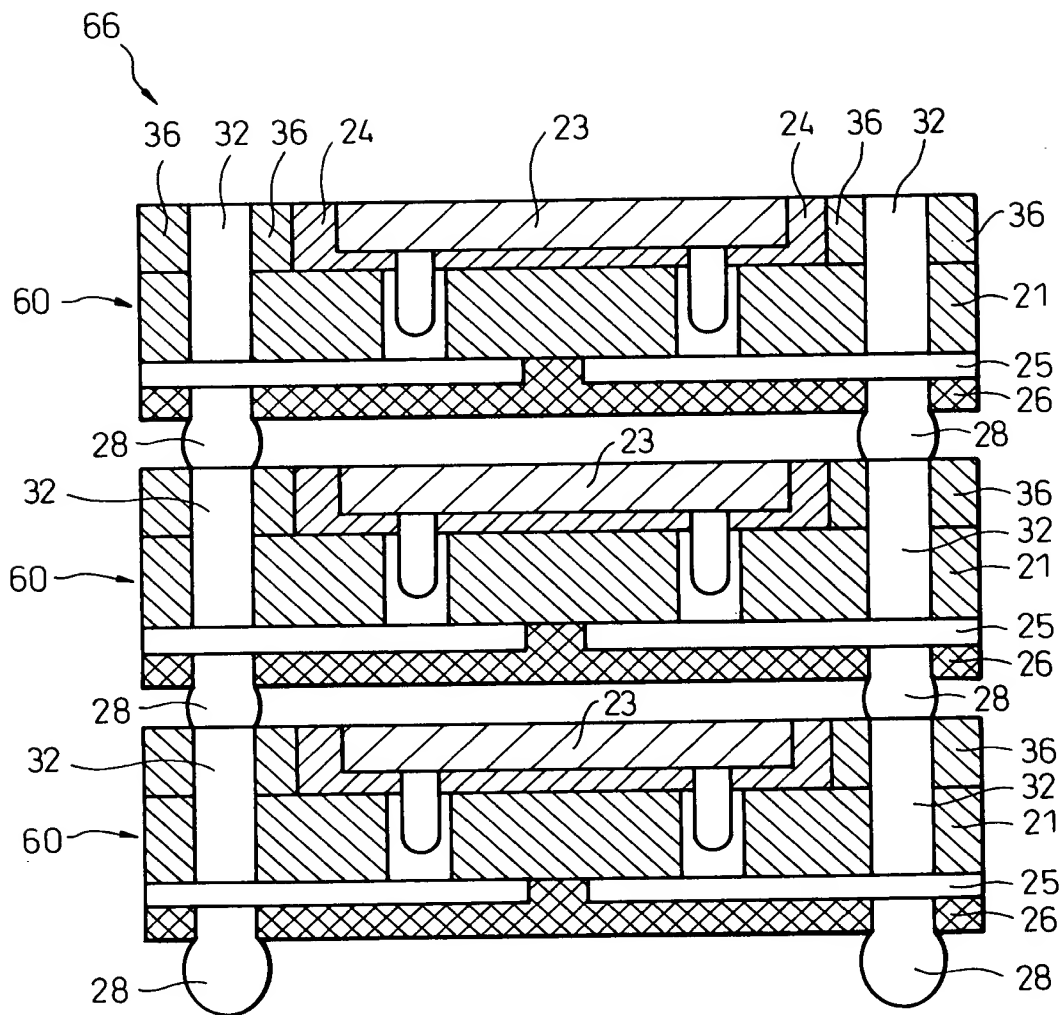
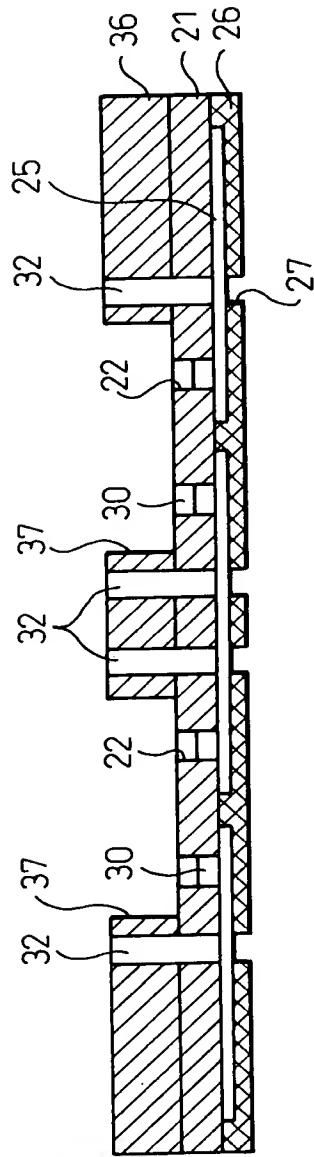


Fig.19



This cross-sectional view shows a central gate structure 23 with a gate dielectric 29 and a gate electrode 37. The gate structure is flanked by side gates 23A and 23B, which also have gate dielectrics 29 and gate electrodes 31. The device is built on a substrate 26, with a channel layer 21 and a source/drain layer 36. A thin layer 27 is on top of the channel layer. The device is surrounded by a passivation layer 30. A dimension G is indicated for the gate structure.

Fig. 21

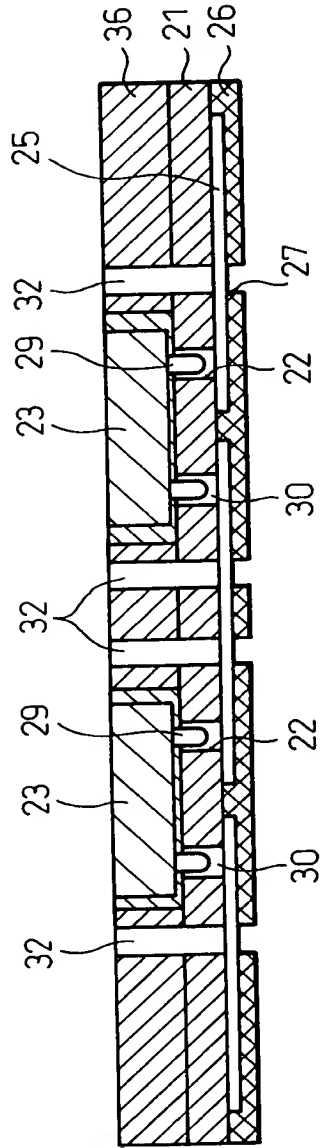


Fig.22

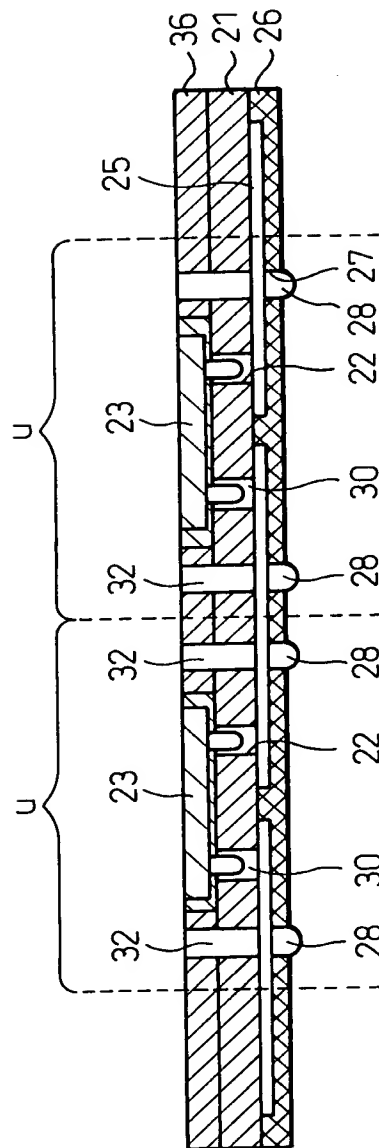
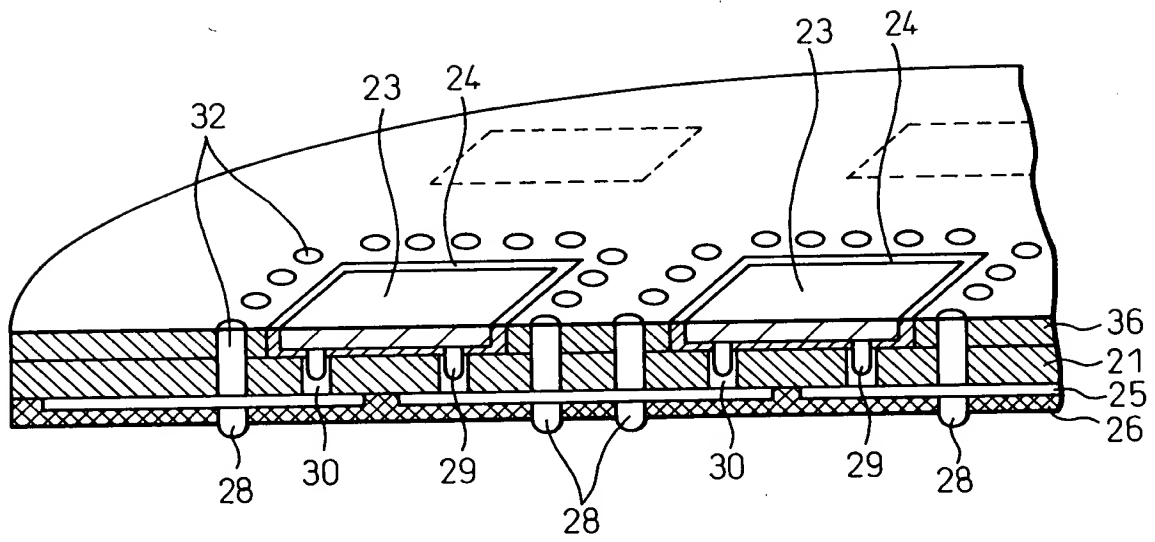
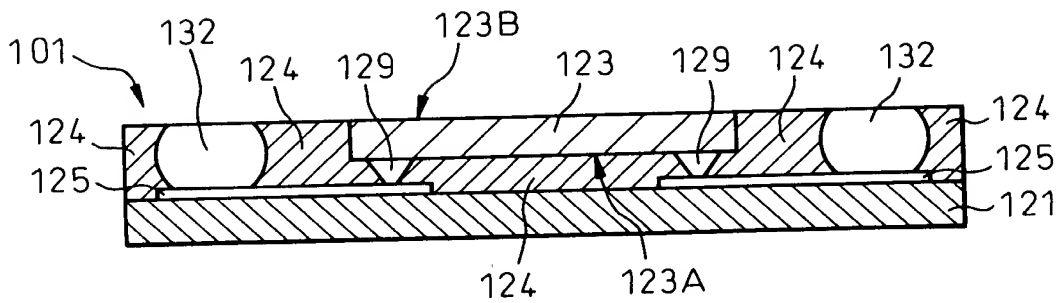


Fig.23

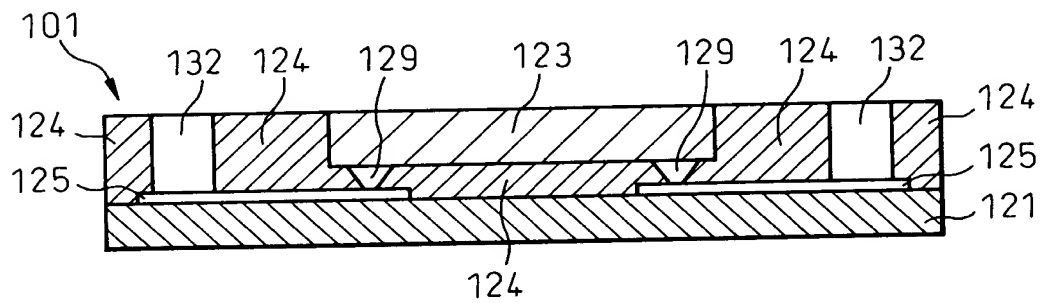


23/34

Fig. 24
(1)



(2)



(3)

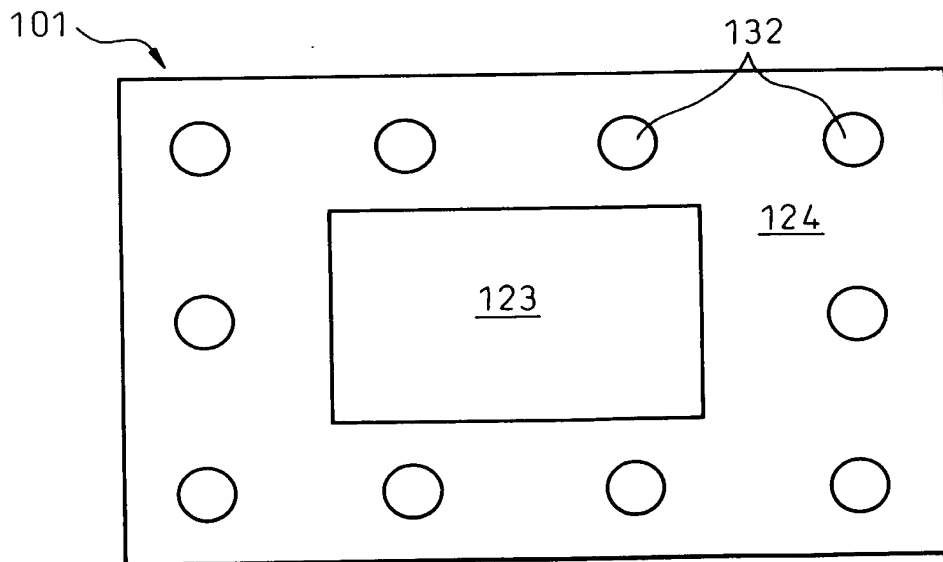


Fig.25

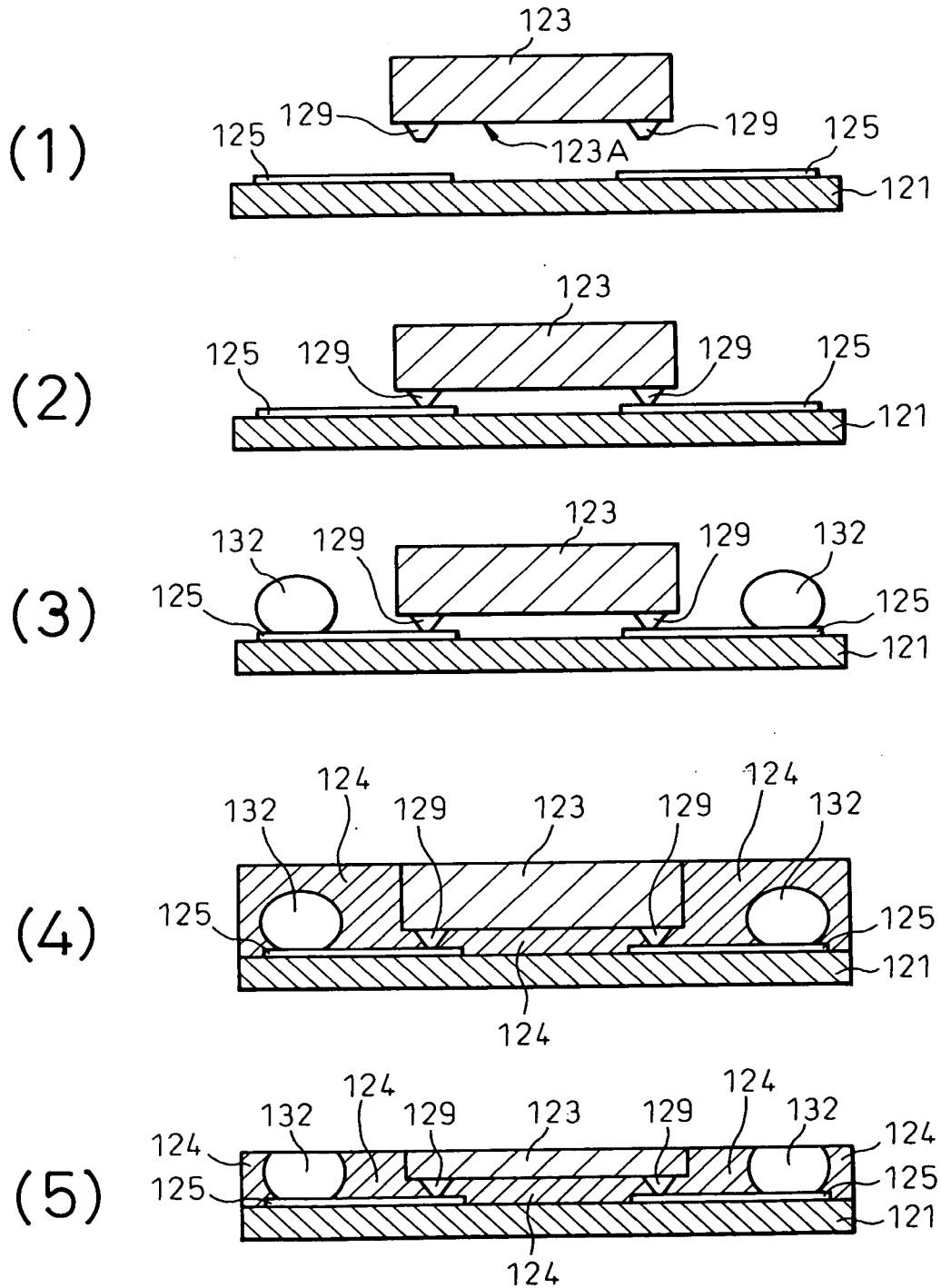
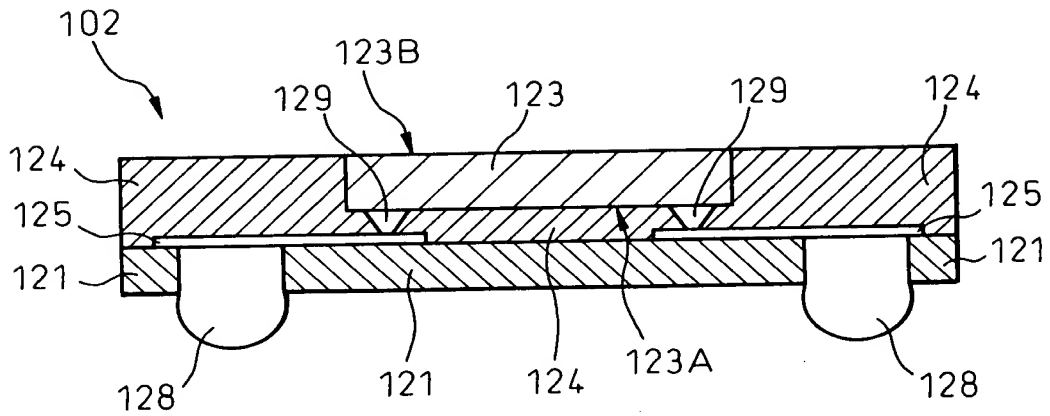


Fig.26

(1)



(2)

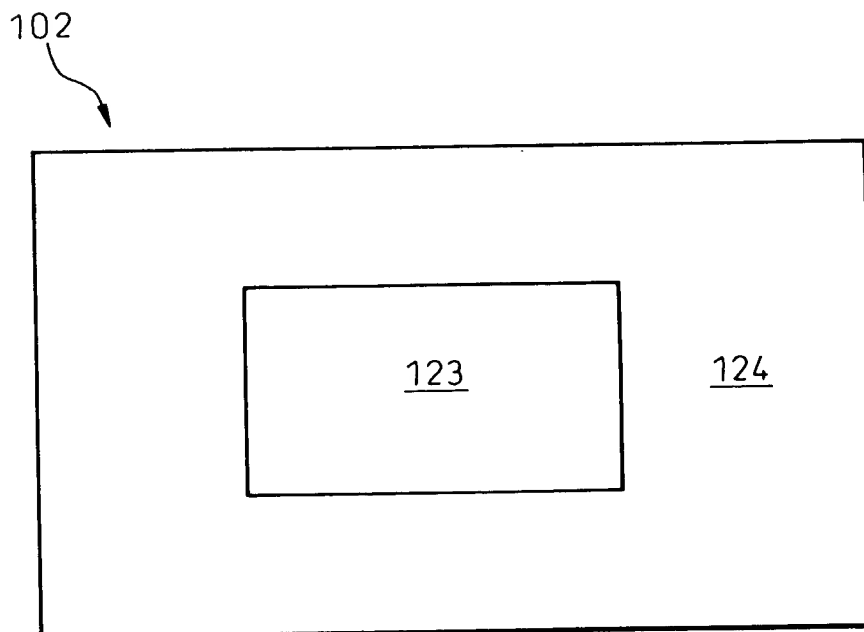


Fig.27

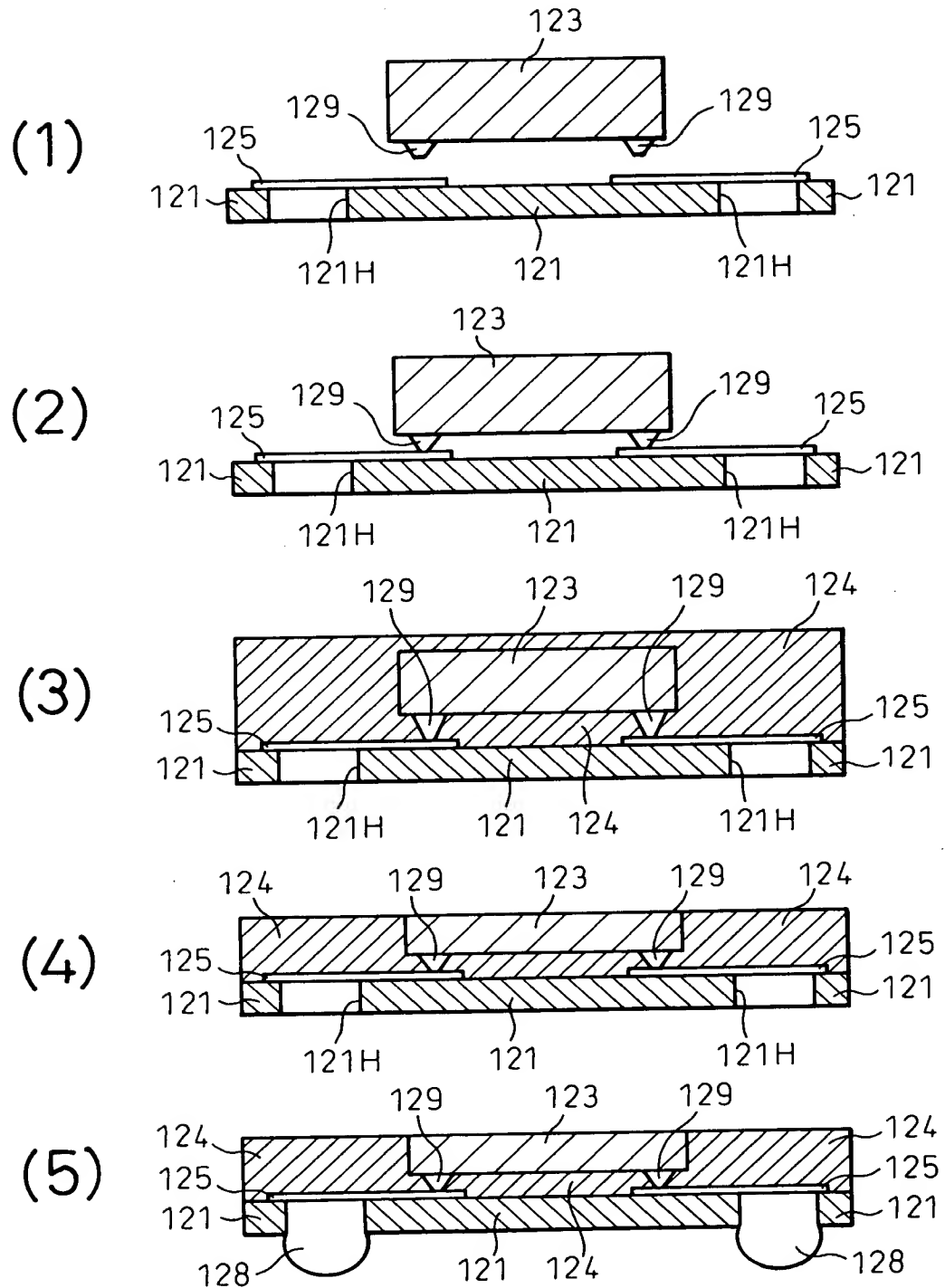
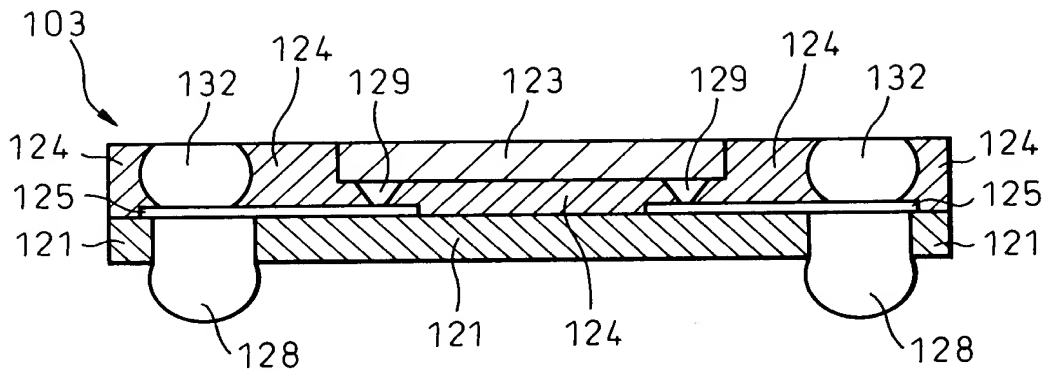


Fig.28

(1)



(2)

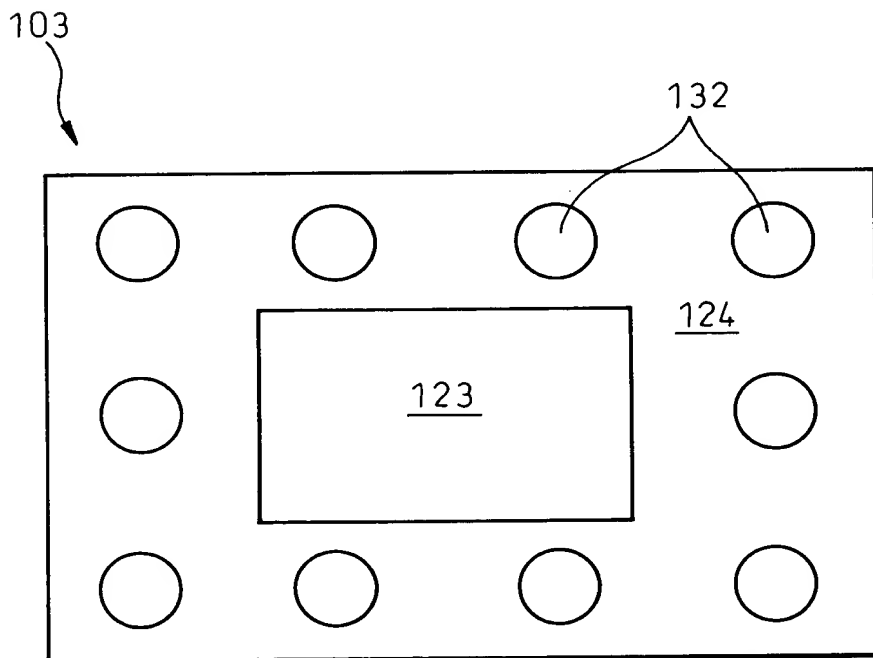
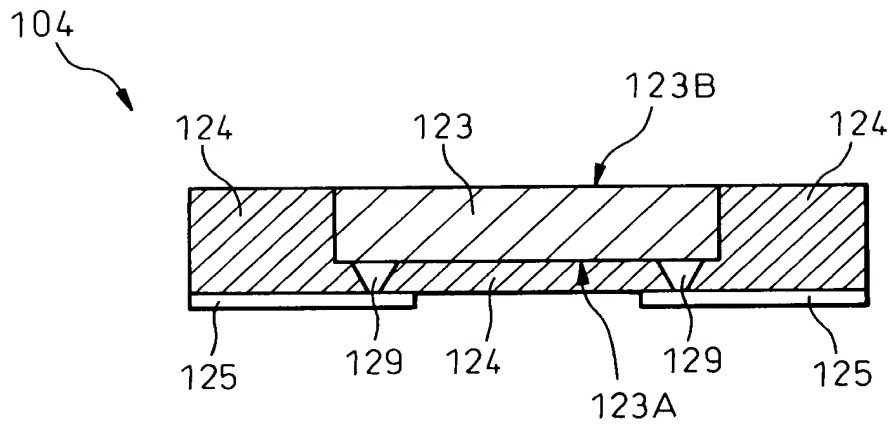


Fig.29

(1)



(2)

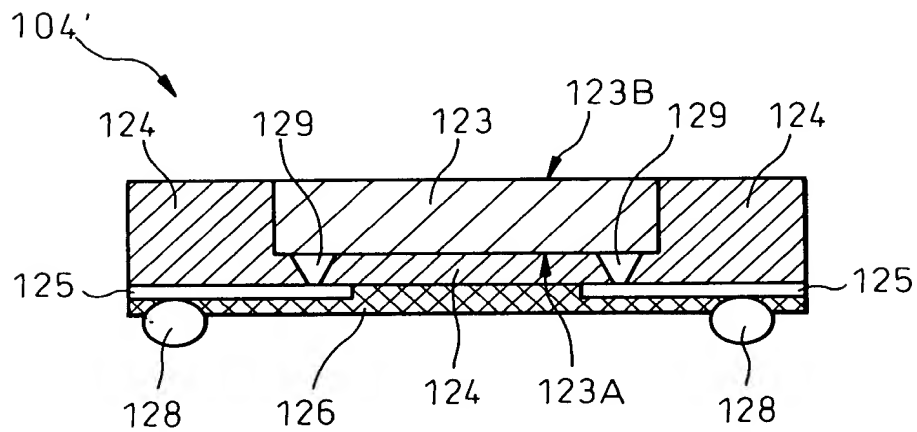


Fig.30

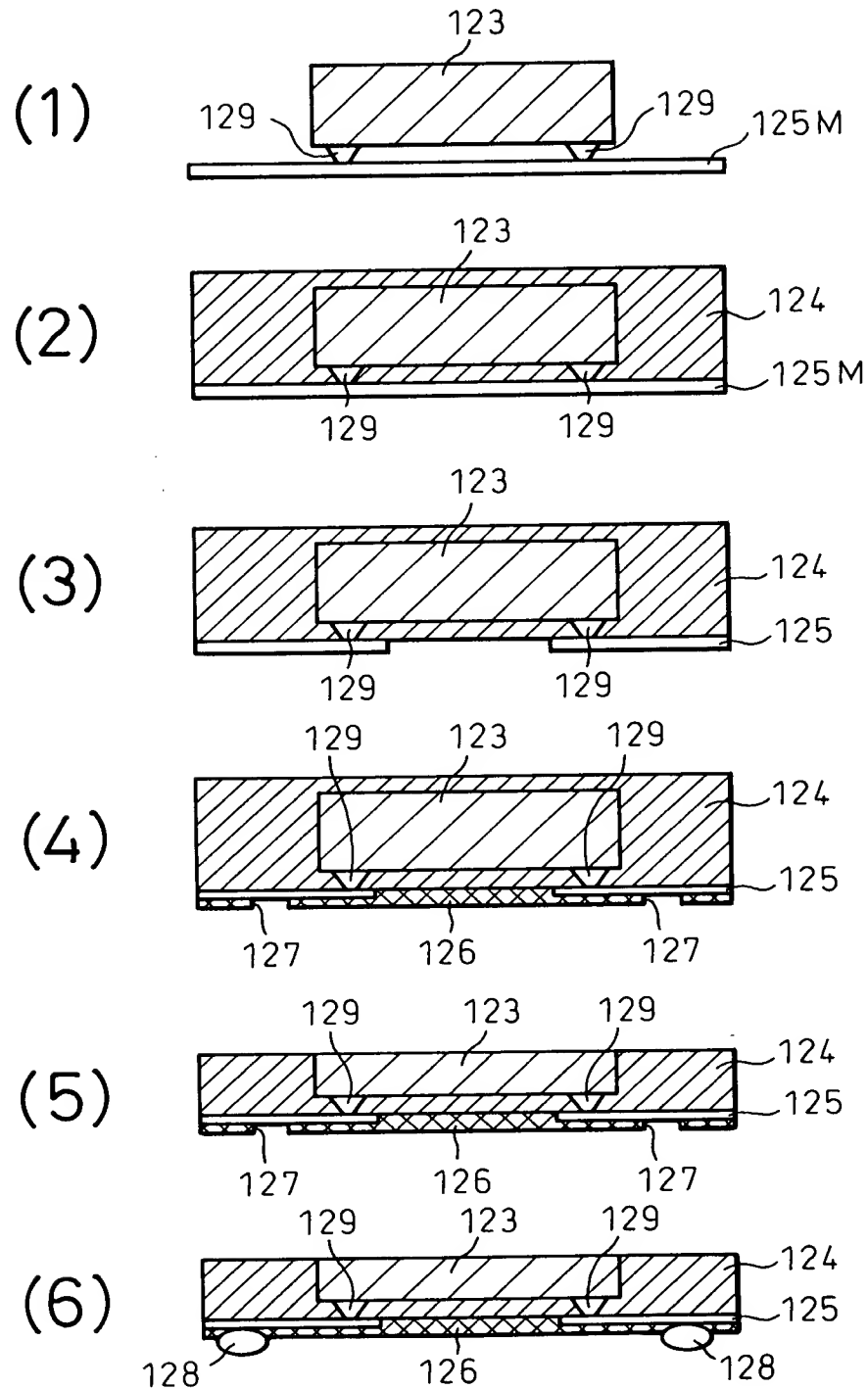


Fig. 31

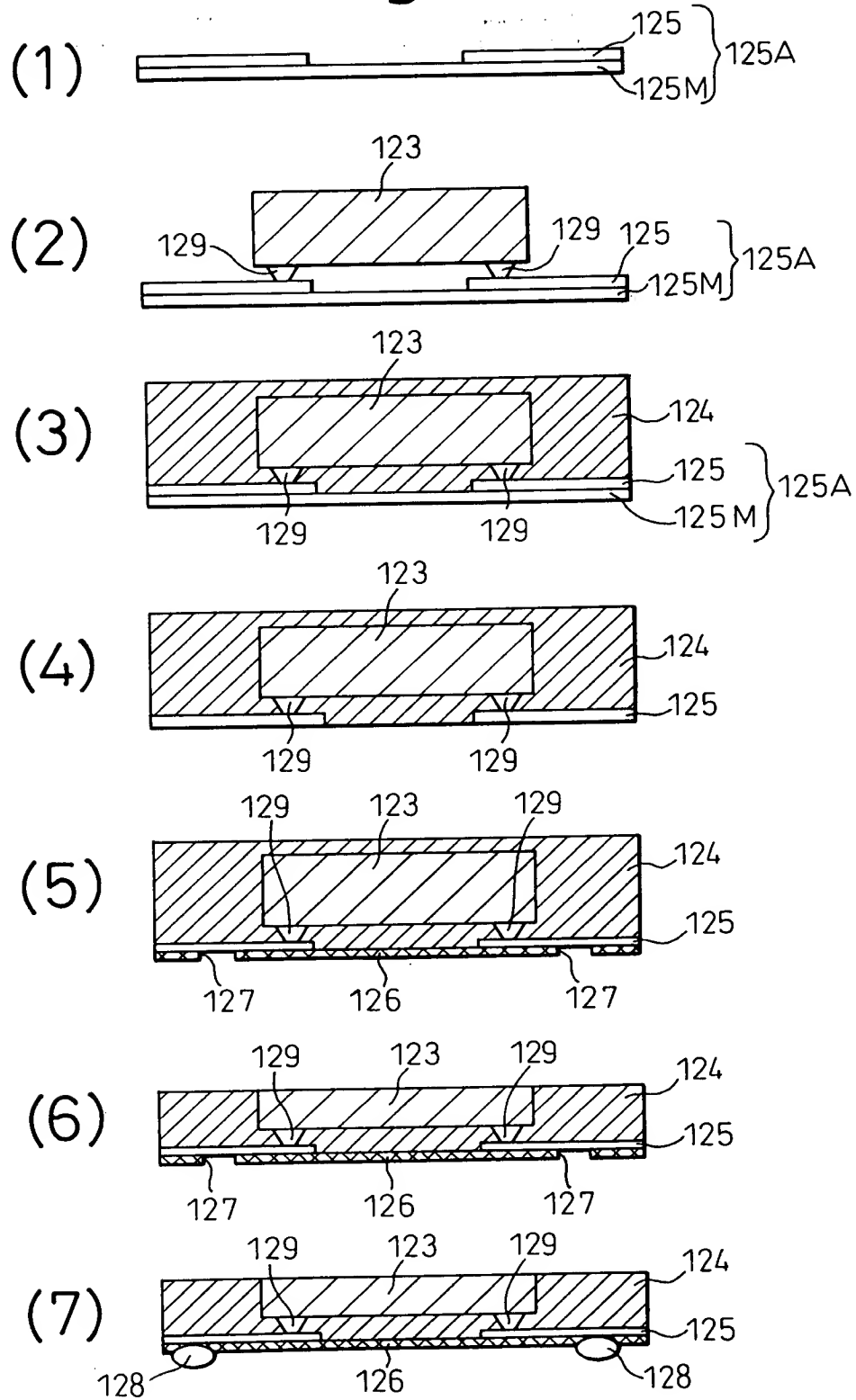
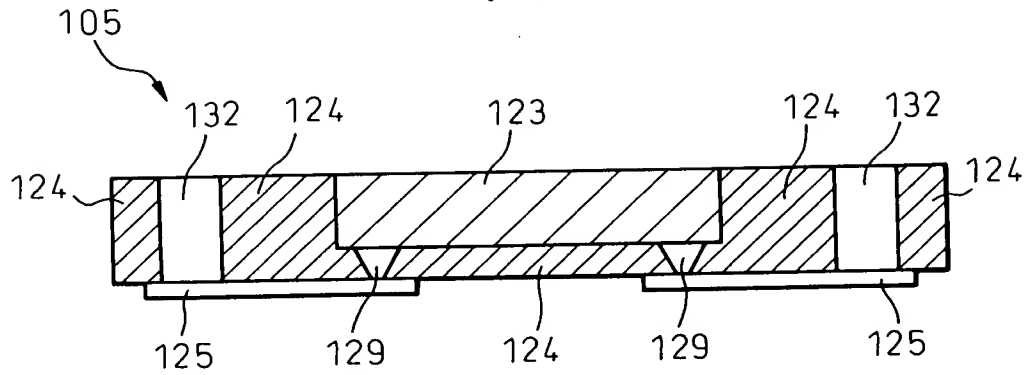
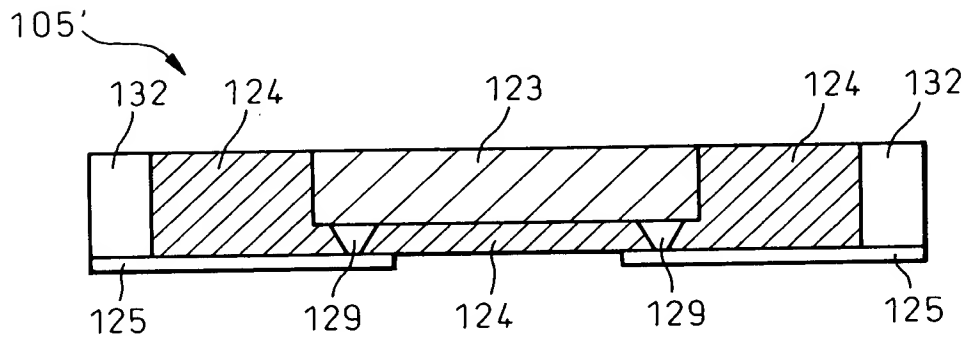


Fig.32

(1)



(2)



(3)

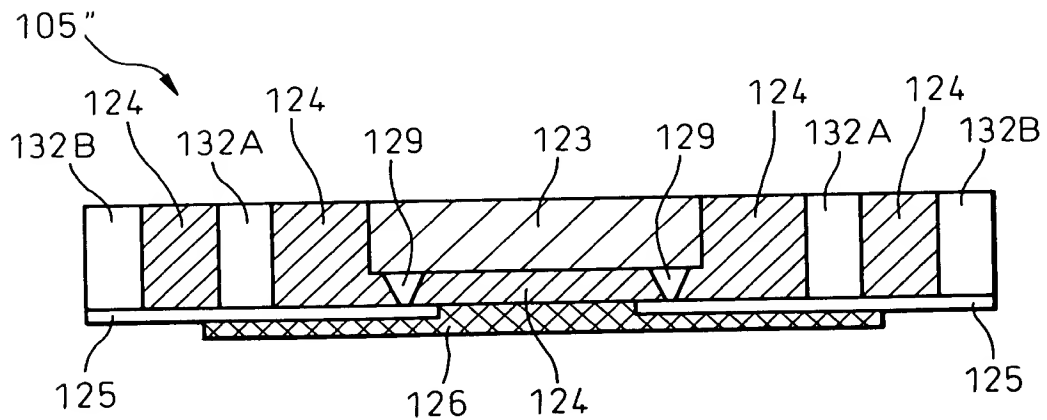


Fig.33

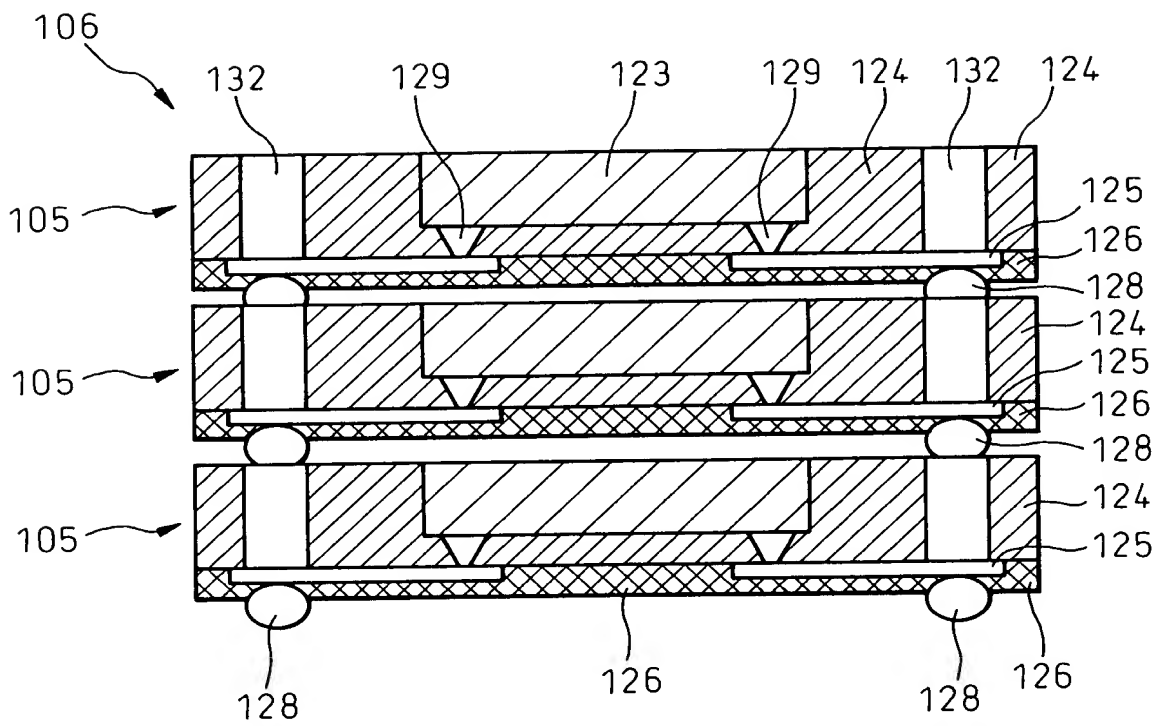
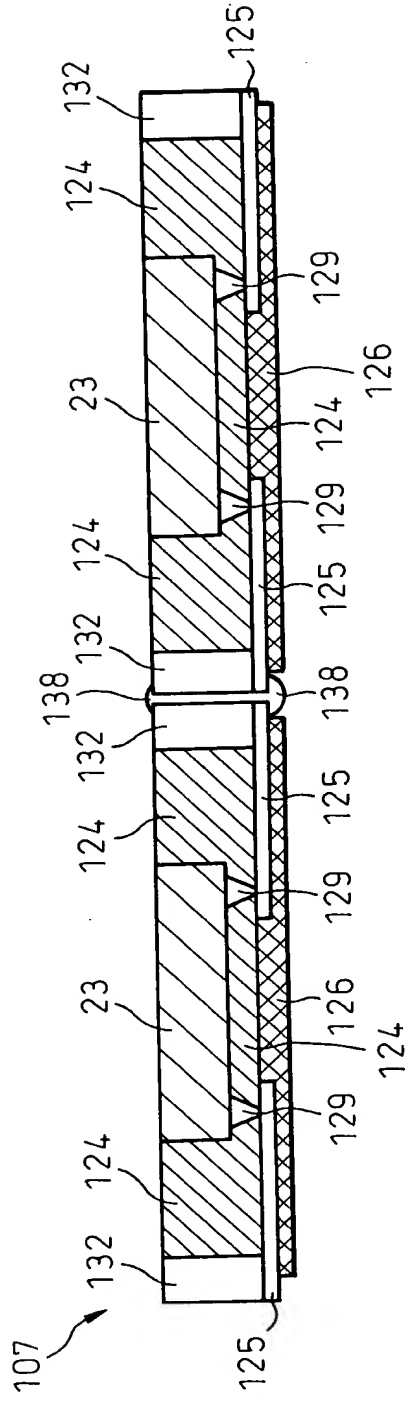


Fig. 34

(1)



(2)

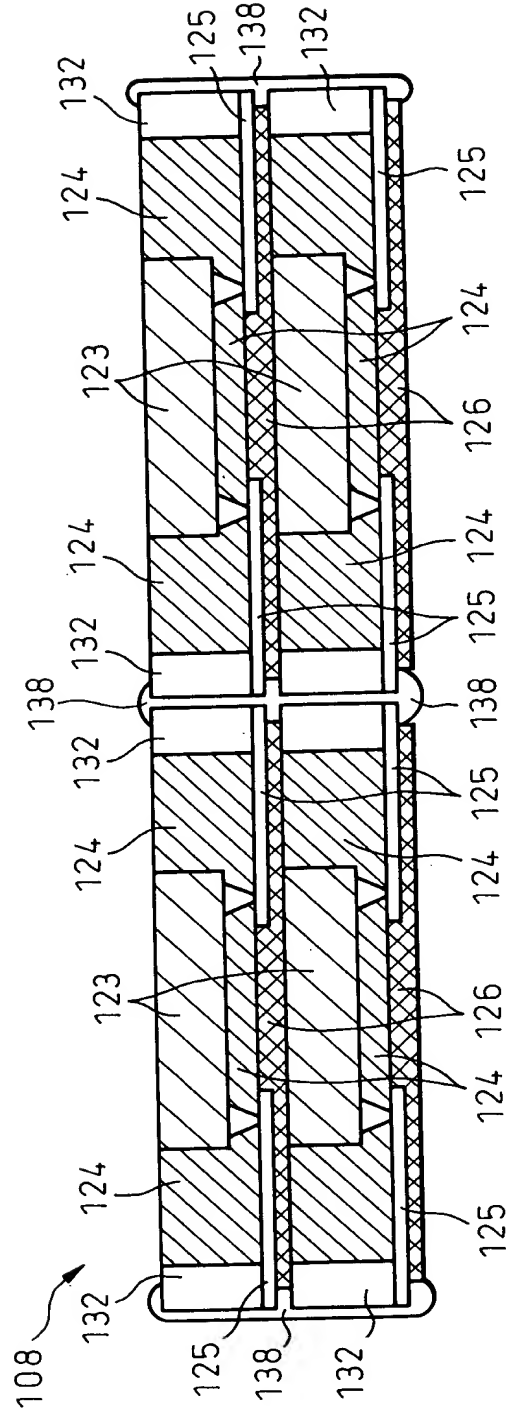
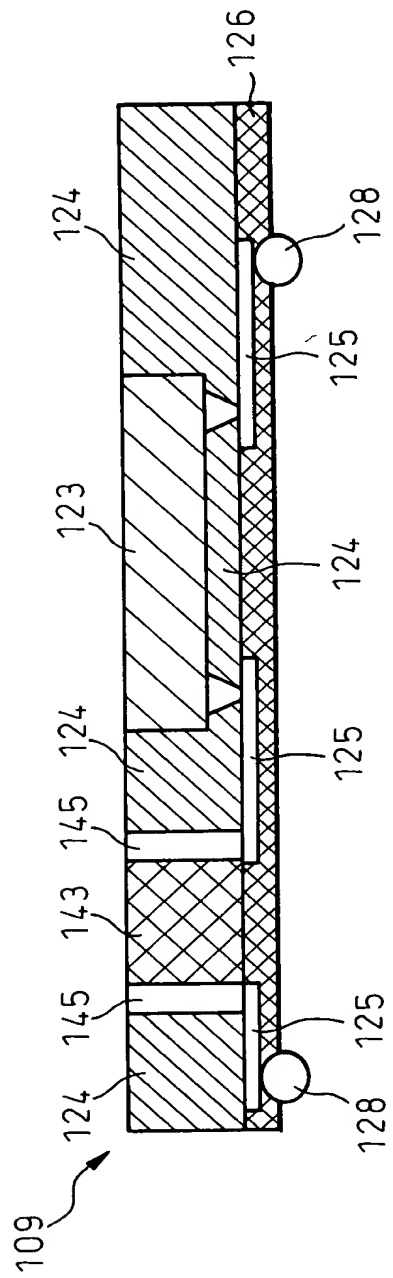


FIG. 35 is a cross-sectional view of a device 109, showing a substrate 124 with a patterned layer 125. The patterned layer 125 includes a central region 123 and side regions 126. A layer 143 is disposed on the substrate 124, and a layer 145 is disposed on the layer 143. A layer 147 is disposed on the substrate 124, and a layer 149 is disposed on the layer 147. A layer 128 is disposed on the substrate 124, and a layer 125 is disposed on the layer 128.

Fig.35

(1)



(2)

